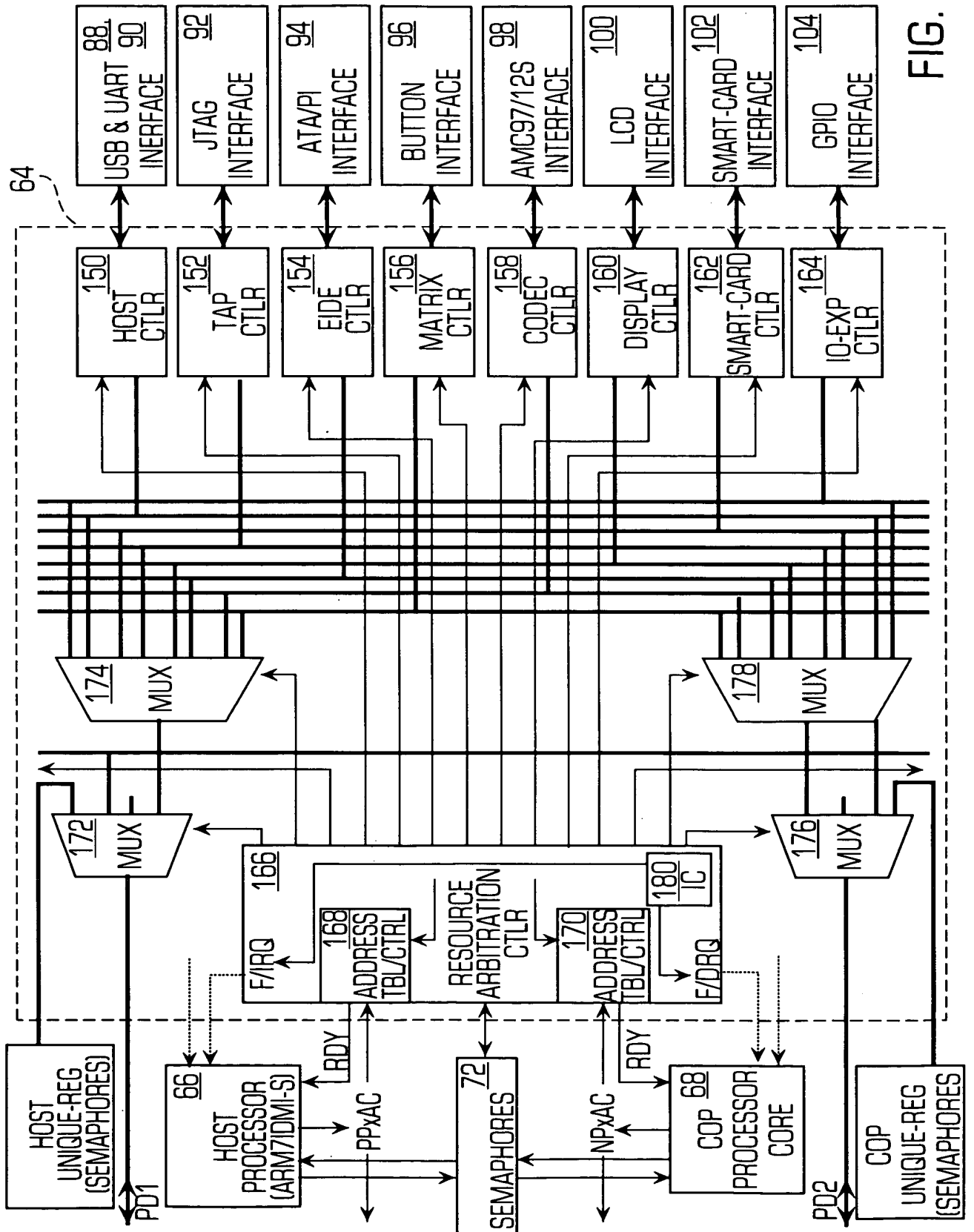
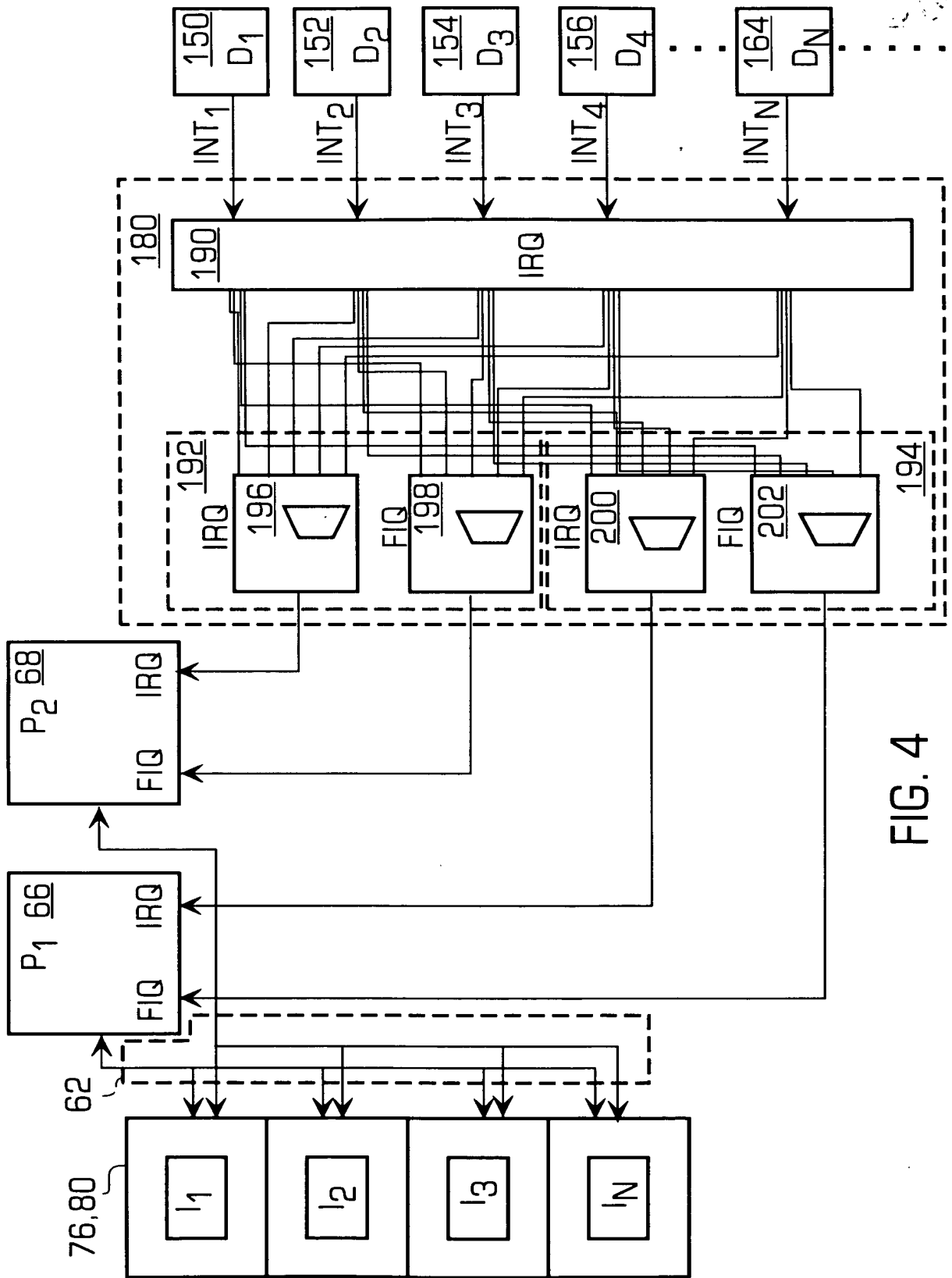


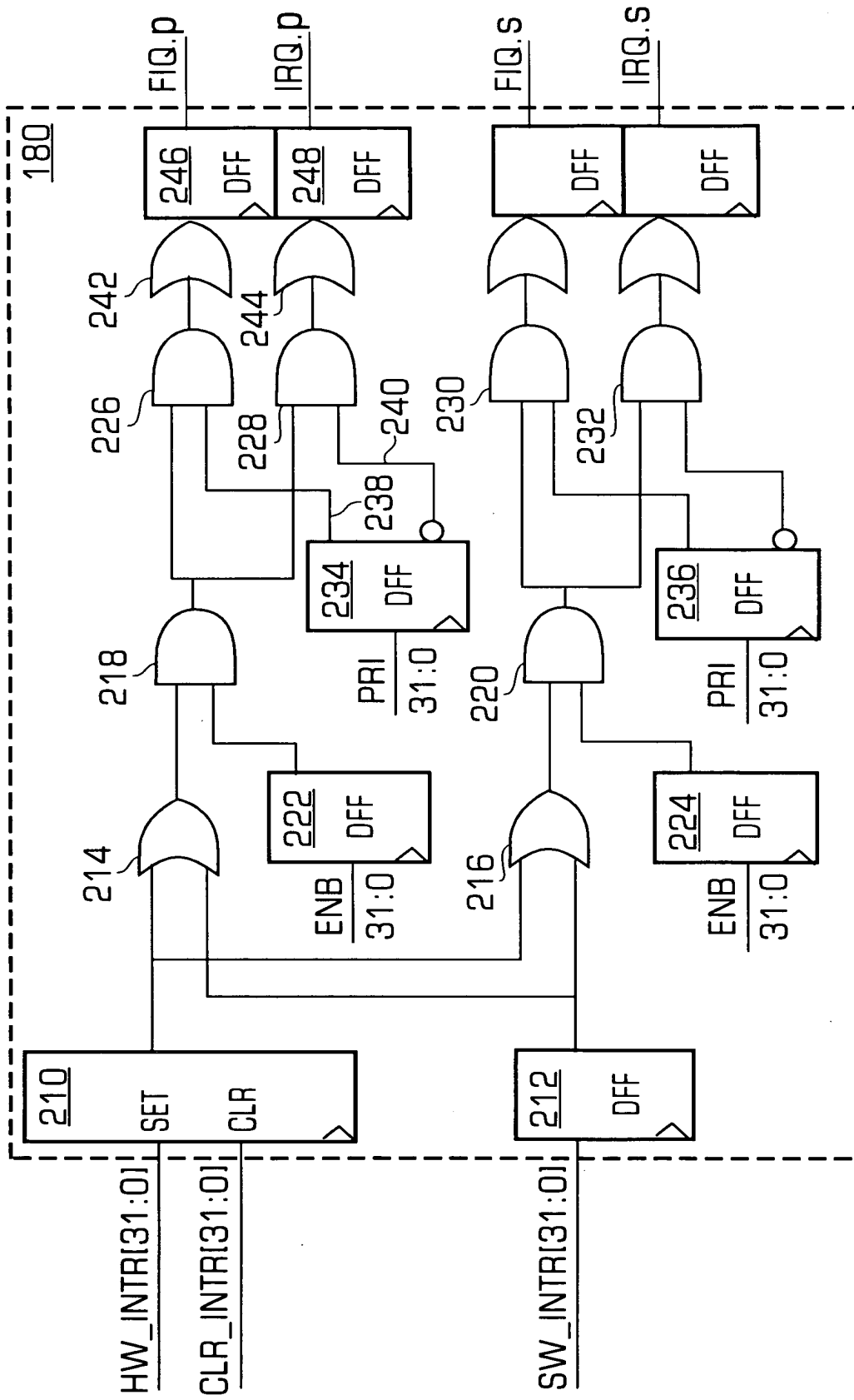
110

112 SYSTEM & USER	114 FIQ	116 SUPERVISOR	118 ABORT	120 IRQ	122 UNDEFINED
r0	r0	r0	r0	r0	r0
r1	r1	r1	r1	r1	r1
r2	r2	r2	r2	r2	r2
r3	r3	r3	r3	r3	r3
r4	r4	r4	r4	r4	r4
r5	r5	r5	r5	r5	r5
r6	r6	r6	r6	r6	r6
r7	r7	r7	r7	r7	r7
r8	r8_fiq	r8	r8	r8	r8
r9	r9_fiq	r9	r9	r9	r9
r10	r10_fiq	r10	r10	r10	r10
r11	r11_fiq	r11	r11	r11	r11
r12	r12_fiq	r12	r12	r12	r12
r13	r13_fiq	r13_svc	r13_abt	r13_irq	r13_und
r14	r14_fiq	r14_svc	r14_abt	r14_irq	r14_und
r15(PC)	r15(PC)	r15(PC)	r15(PC)	r15(PC)	r15(PC)

FIG. 2







FUNCTIONAL BLOCK DIAGRAM OF INTERRUPT CONTROLLER

FIG. 5

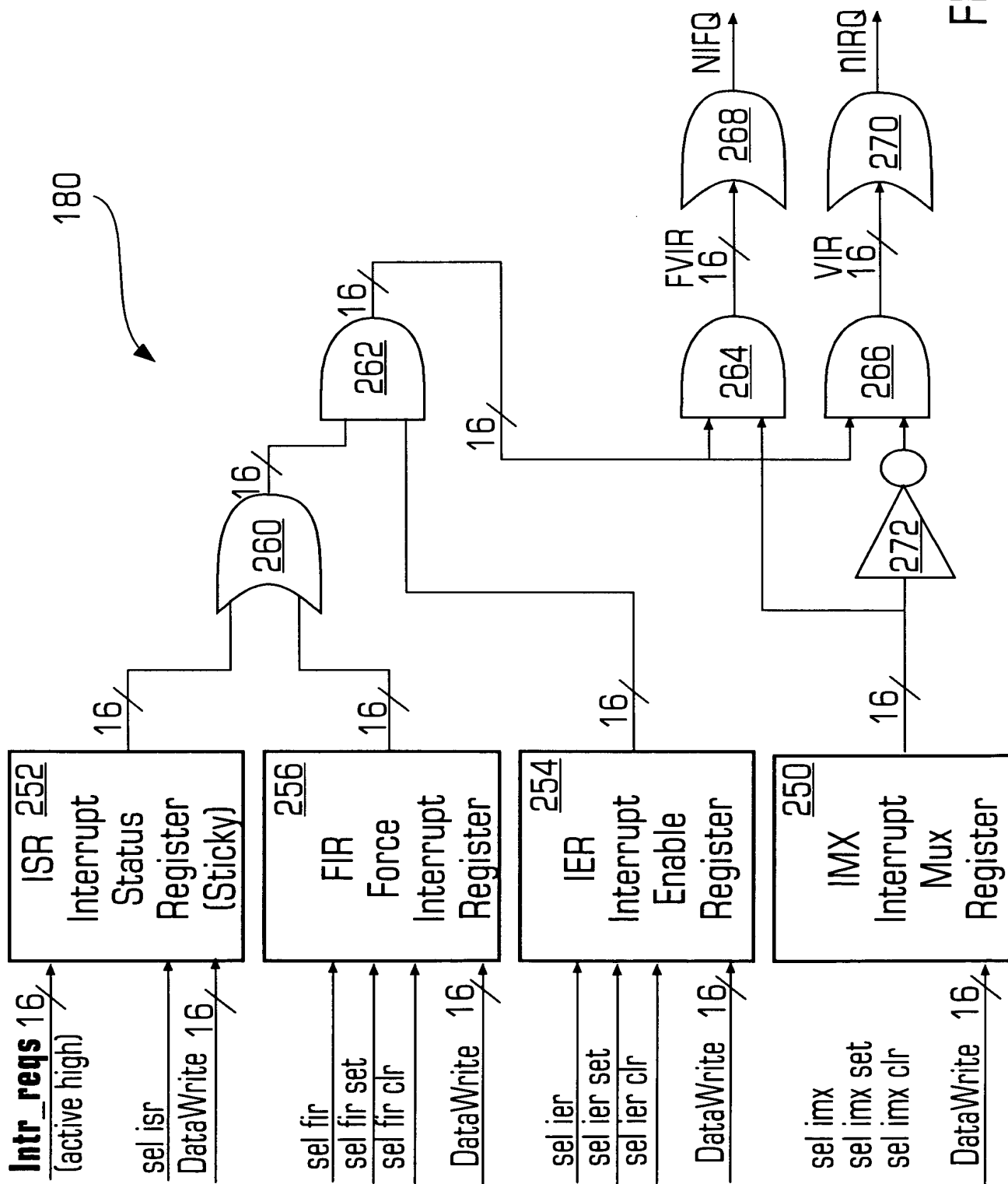


FIG. 6

280



Offset	Register	Description
0	ISR	Interrupt Status Register
4	IER	Interrupt Enable Register
8	IER_set	Each bit written as one will set the corresponding bit in IER
C	IER_clr	Each bit written as one will clr the corresponding bit in IER
10	FIR	Force Interrupt Register
14	FIR_set	Each bit written as one will set the corresponding bit in FIR
18	FIR_clr	Each bit written as one will clr the corresponding bit in FIR
1C	IMX	Interrupt Mux Register ('1/0' Routes interrupt to nFIQ/nIRQ)
20	IMX_set	Each bit written as one will set the corresponding bit in IMX
24	IMX_clr	Each bit written as one will clr the corresponding bit in IMX
28	VIR	Read only Valid Interrupt Register for nIRQ
2C	FVIR	Read only Fast Valid Interrupt Register for nFIQ

282

284

FIG. 7

8/11

Bit	Description
0	USB
1	UART A
2	UART B
3	External
4	USB Fast
5	Not Defined (CIF)
6	Not Defined
7	Not Defined (Keyboard)
8	EIDE 1
9	EIDE 2
A	Not Defined
B	Not Defined
C	Not Defined
D	Timer 2
E	Timer 1
F	Not defined
10	USB Reset
11	AC
12	Timer 1
13	Timer 2
31:14	Not Defined

FIG. 8

FIG. 9A

FIG. 9A

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10/11

[illegible]



IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
IRQ15	IRQ14	IRQ13	IRQ12	IRQ11	IRQ10	IRQ9	IRQ8	IRQ7	IRQ6	IRQ5	IRQ4	IRQ3	IRQ2	IRQ1	IRQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
FIQ15	FIQ14	FIQ13	FIQ12	FIQ11	FIQ10	FIQ9	FIQ8	FIQ7	FIQ6	FIQ5	FIQ4	FIQ3	FIQ2	FIQ1	FIQ0
ISR15	ISR14	ISR13	ISR12	ISR11	ISR10	ISR9	ISR8	ISR7	ISR6	ISR5	ISR4	ISR3	ISR2	ISR1	ISR0
FIR15	FIR14	FIR13	FIR12	FIR11	FIR10	FIR9	FIR8	FIR7	FIR6	FIR5	FIR4	FIR3	FIR2	FIR1	FIR0
FIR SET (SET FORCED INTERRUPT BIT)															
FIR CLR (CLEAR FORCED INTERRUPT BIT)															
IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
CPU_IER_SET (ENABLE INTERRUPT SOURCE FOR CPU)															
CPU_IER_CLR (DISABLE INTERRUPT SOURCE FOR CPU)															
CPU_IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR CPU)															
IER15	IER14	IER13	IER12	IER11	IER10	IER9	IER8	IER7	IER6	IER5	IER4	IER3	IER2	IER1	IER0
COP_IER_SET (ENABLE INTERRUPT SOURCE FOR COP)															
COP_IER_CLR (DISABLE INTERRUPT SOURCE FOR COP)															
COP_IEP_CLASS (SET PRIORITY INTERRUPT SOURCE FOR COP)															
DMA_SOURCE_STATUS															

FIG. 9C